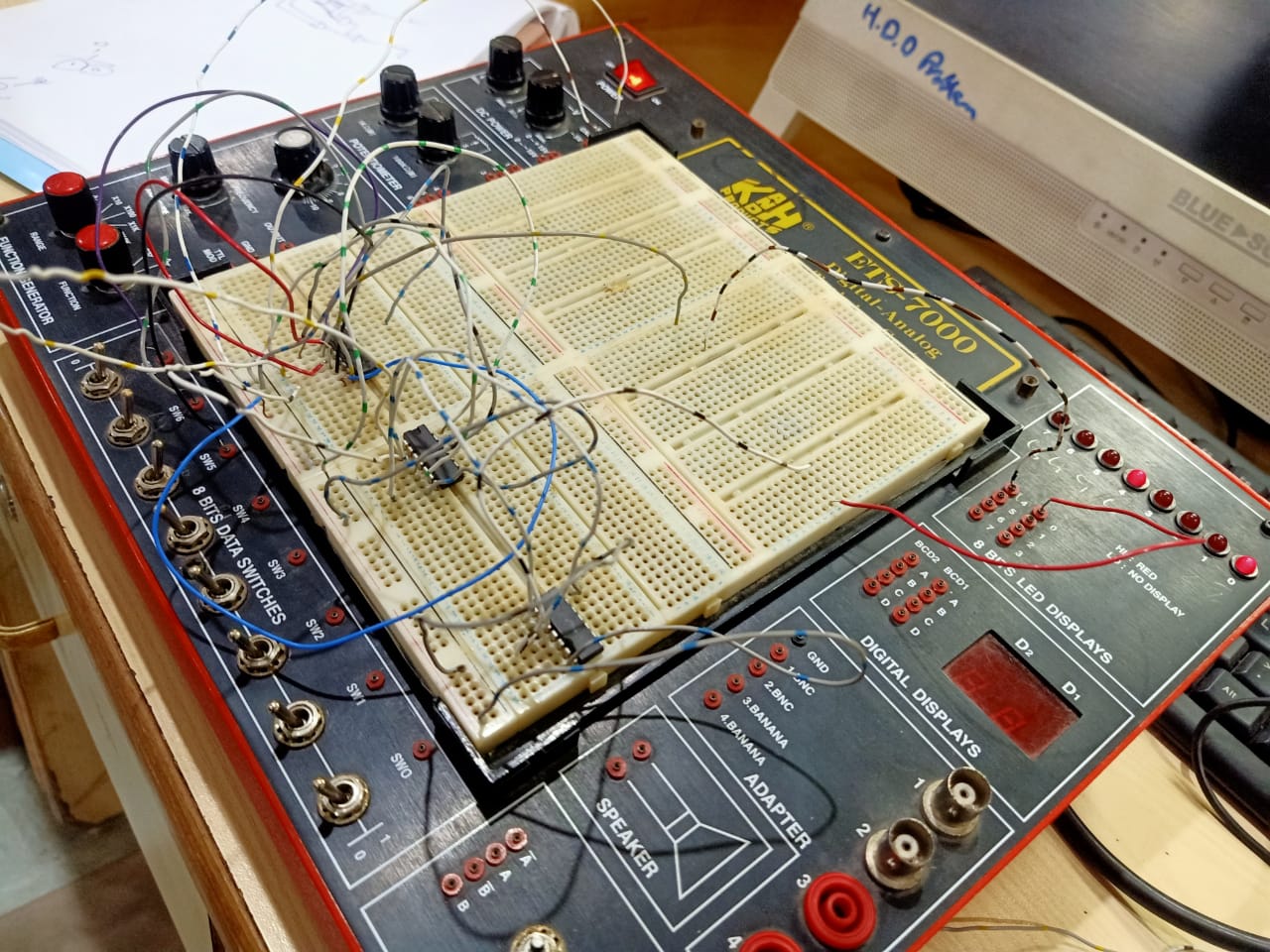
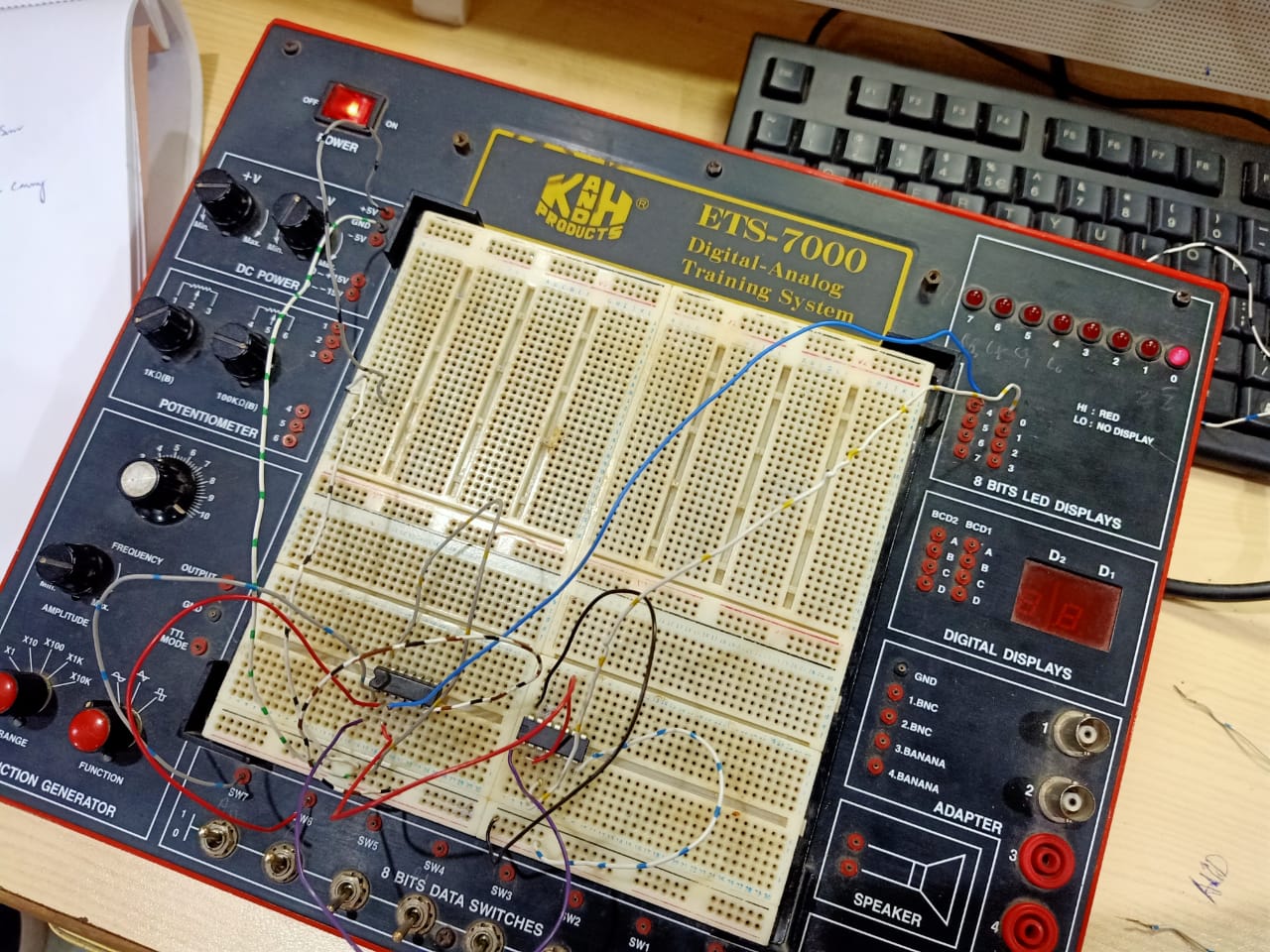
Roll no- 20k-0409

Name: Mukand Krishna

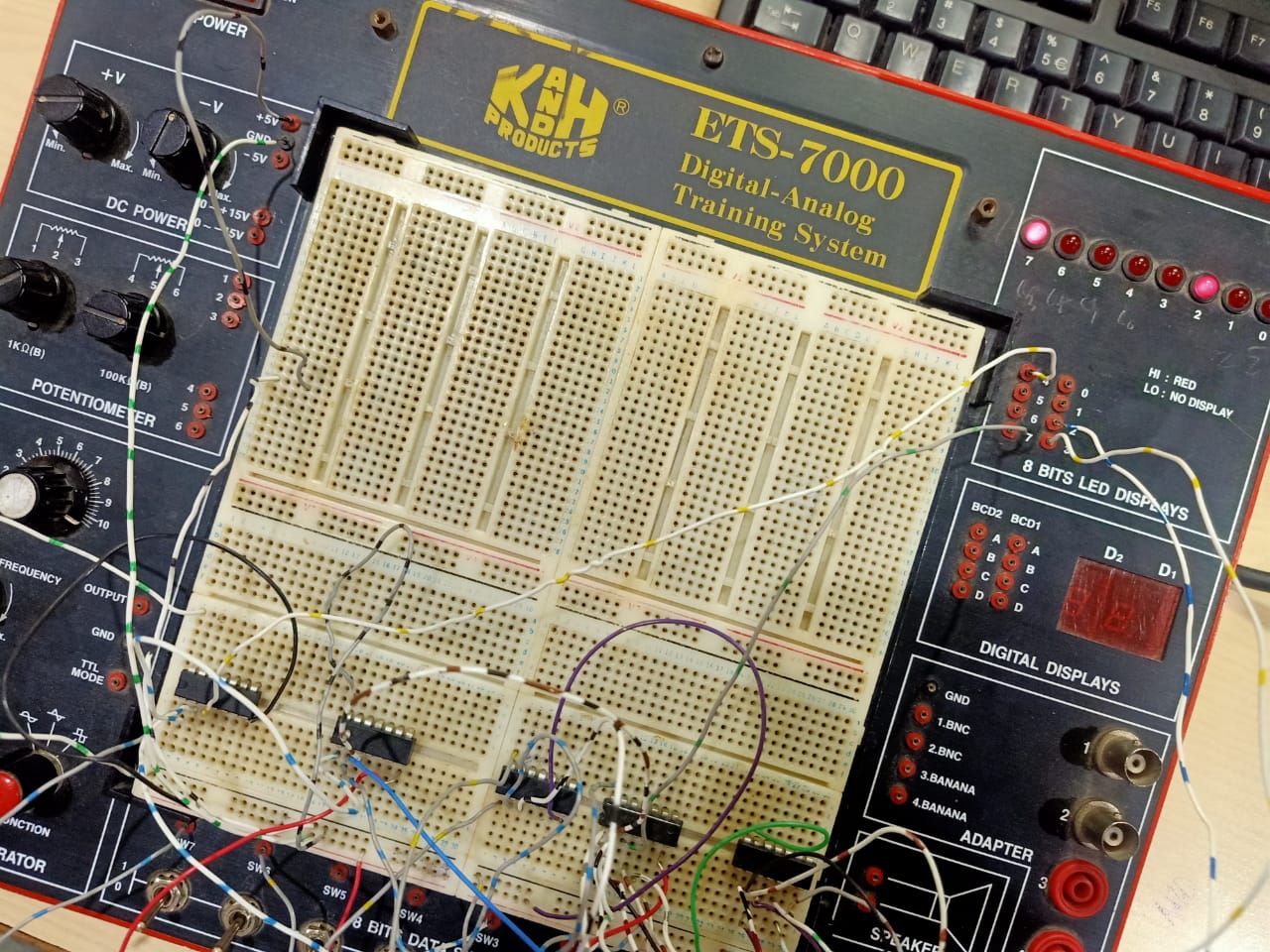
**Q 1 - Full adder circuit.**



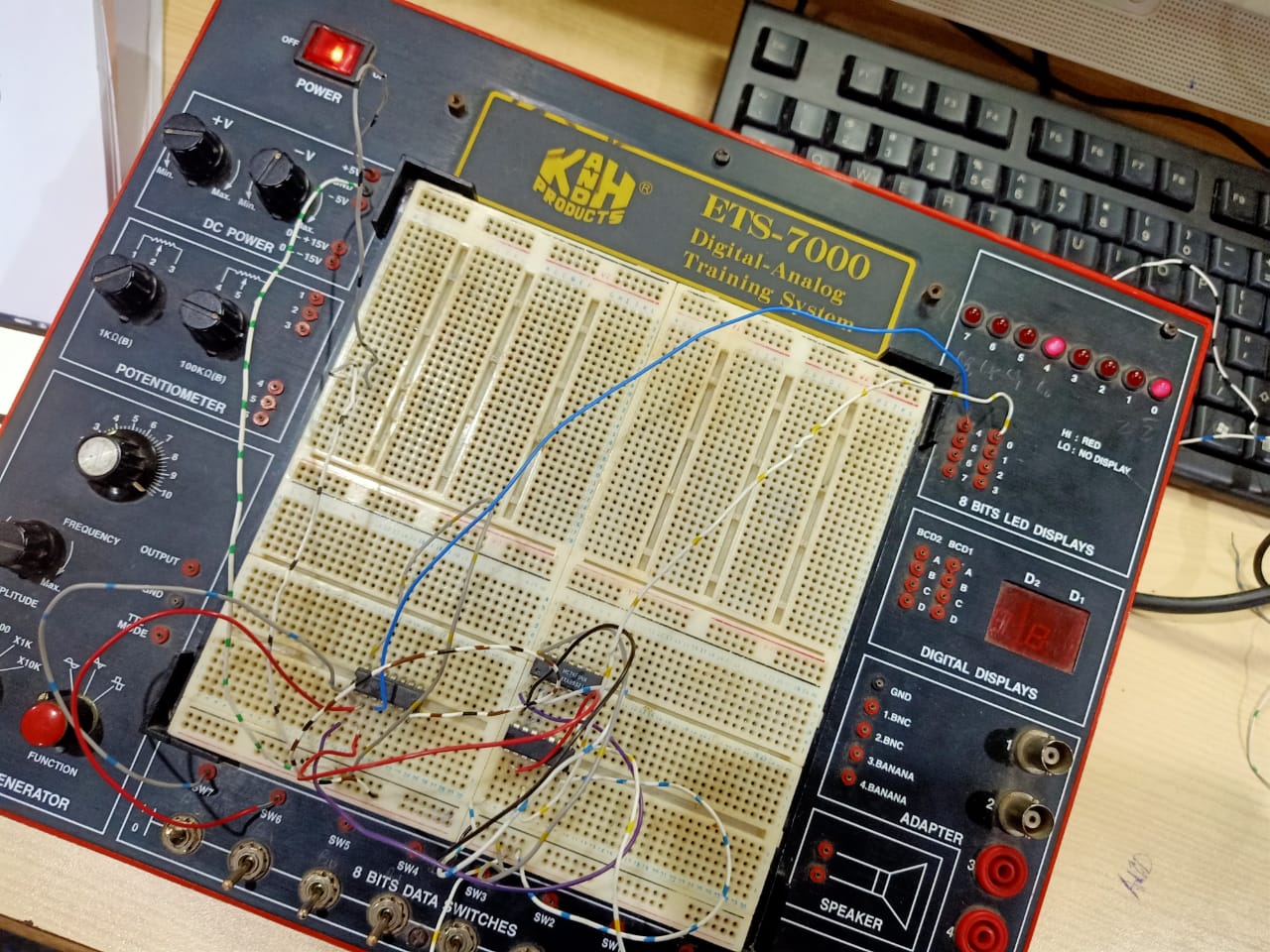
**Q 2 – Half adder circuit**



**Q 3 – 2\*2 Bit Multiplier**

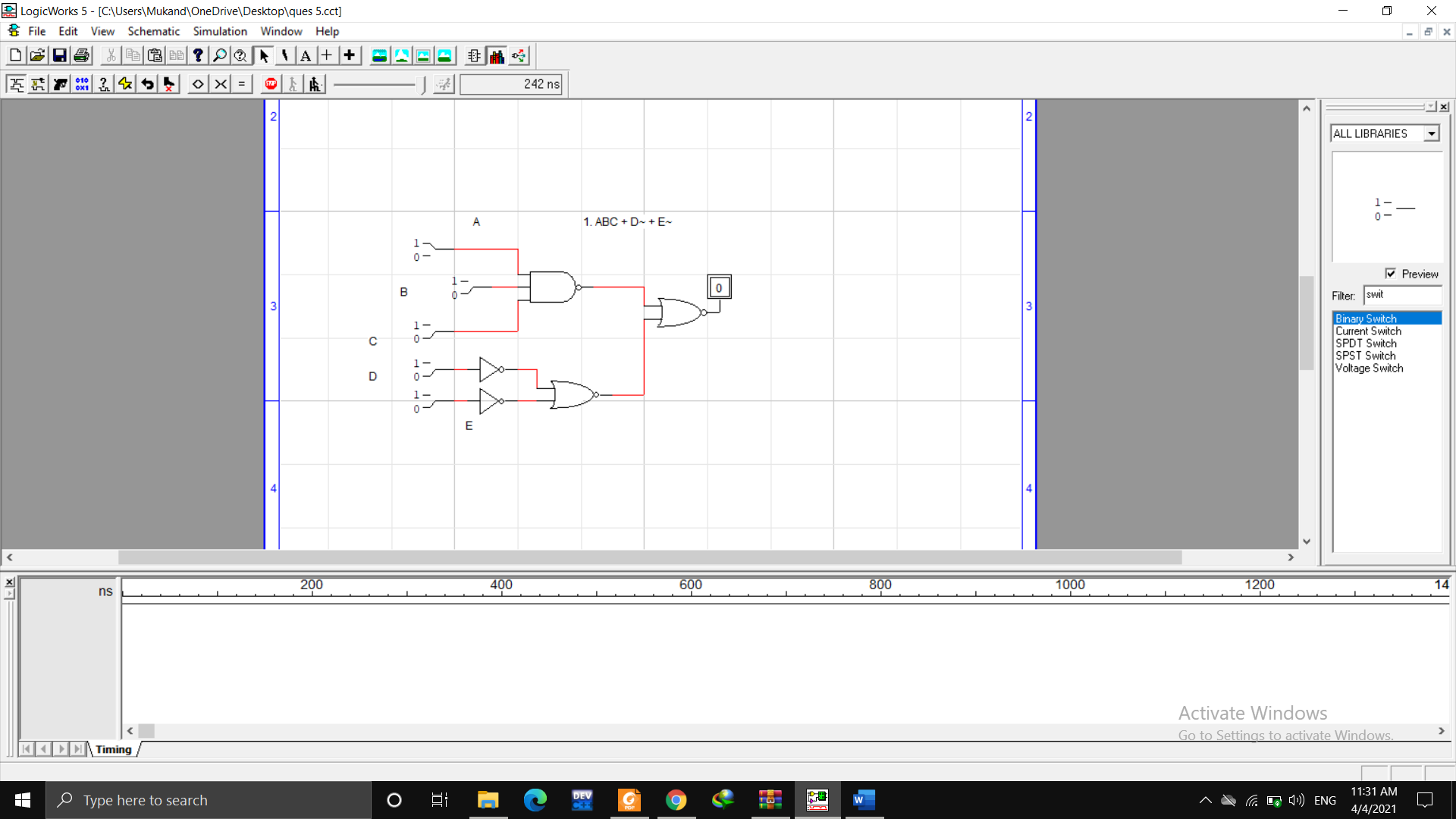


**Q 4 – Half Subtractor**



**Q5.** Design circuit on trainer for given expressions by using either NAND or NOR gate

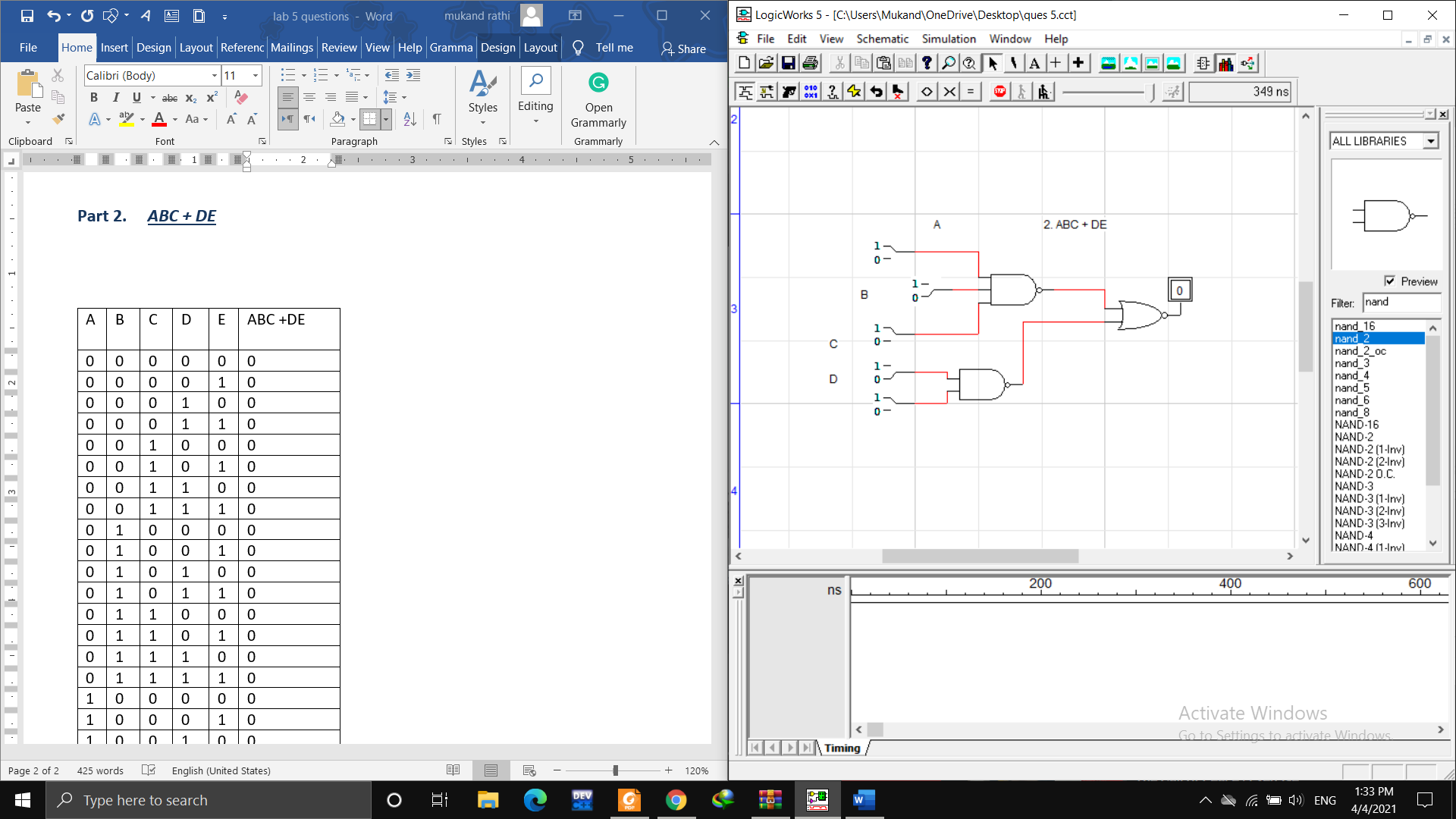
**Part 1** ***ABC + D~ + E~***



|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | C | D | E | ABC +D~+E~ |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |

**Part 2. *ABC + DE***

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | C | D | E | ABC +DE |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |



**Q 6** Use a Karnaugh map to minimize the following standard SOP expression and design circuit on trainer.

**AB~C + A~BC + A~B~C + A~B~C~ + AB~C~**

**Positioning 1’s** in the k map

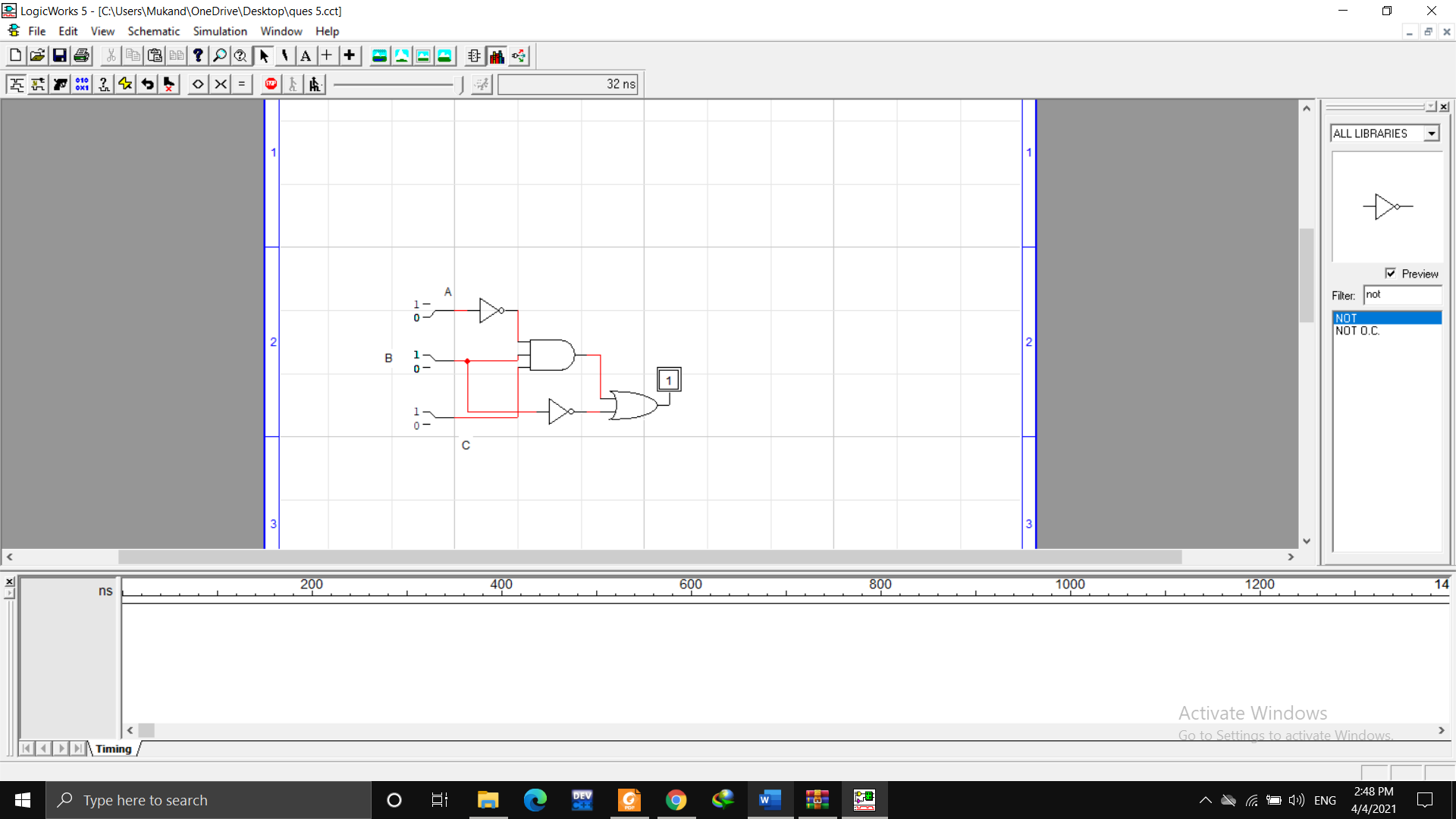
B~C~ B~C BC BC~

|  |  |  |  |
| --- | --- | --- | --- |
| **1** | **1** | 1 |  |
| **1** | **1** |  |  |

A~

A

**Simplified expression:**  **B~ + A~BC**



**Q7.** Use a Karnaugh map to minimize the following standard POS expression and design circuit on trainer.

**(B + C + D) (A + B + C~ + D) (A~ + B + C + D~) (A~ + B + C + D~) (A + B~ + C + D) (A~ + B~ + C + D)**

**(AA~ + B + C + D) (A + B + C~ + D) (A~ + B + C + D~) (A~ + B + C + D~) (A + B~ + C + D) (A~ + B~ + C + D)**

**(A + B + C + D) (A~ + B + C + D) (A + B + C~ + D) (A~ + B + C + D~) (A~ + B + C + D~) (A + B~ + C + D) (A~ + B~ + C +**

**Positioning 0’s** in the k map

|  |  |  |  |
| --- | --- | --- | --- |
| **0** | **0** |  |  |
| **0** | **0** |  | 0 |
|  |  |  |  |
| 0 |  |  |  |

C+DC+D ~ C~+D~ C~+D

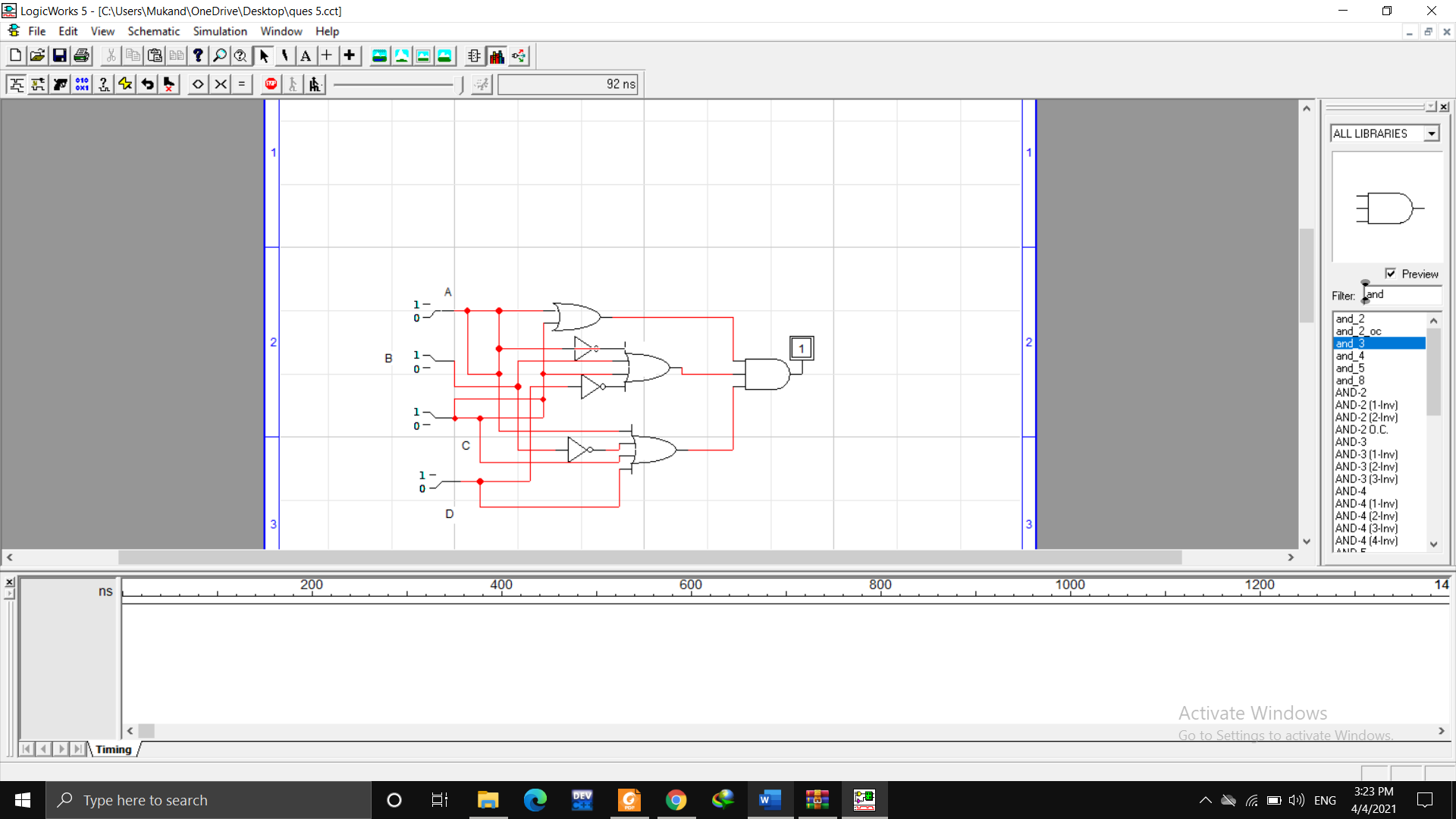
A+B

A+B~

A~+B~

A~+B

**Simplified expression: (A + C) (A~ + B + C + D~) (A + B~ + C + D)**

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